PR6232

High Precision CC/CV Primary-Side PWM Power Controller

Features

- Up to 5% Precision for Constant Voltage Regulation and Constant Current Regulation at Universal AC input
- Primary-side Sensing and Regulation Without TL431 and Opto-coupler
- Flyback Topology In DCM Operation
- Soft-start
- Built-in Leading Edge Blanking (LEB)
- Frequency Jitter to Reduce System EMI
- Programmable CV and CC Regulation
- Adjustable Constant Current and Output Power Setting
- Built-in Secondary Constant Current Control with Primary Side Feedback
- Built-in Secondary Constant Voltage Sampling Controller
- Program Cable Drop Compensation
- Rich Protections For System Reliability including
  - VDD Under Voltage Lockout with Hysteresis (UVLO)
  - Cycle-by-Cycle Current Limiting and Peak Current Protection (OCP)
  - VDD Over Voltage Protection (OVP)
  - VDD Clamp
- Lead-free SOT23-6 package

Applications

- Cell Phone /Digital Cameras Charger
- Small Power Adaptor
- Auxiliary Power for PC, TV etc.
- Linear Regulator/RCC Replacement

General Description

PR6232 is a high performance offline PWM power controller for low power AC/DC charger and adaptor applications. It operates in primary-side sensing and provides constant voltage (CV) and constant current (CC) regulation without TL431 and opto-coupler. A typical output CC/CV curve is shown as in the Fig.1.

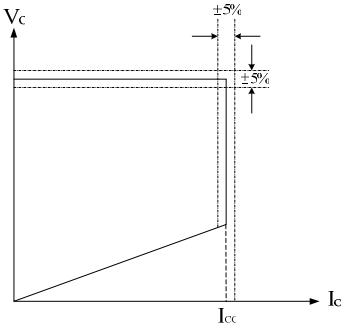
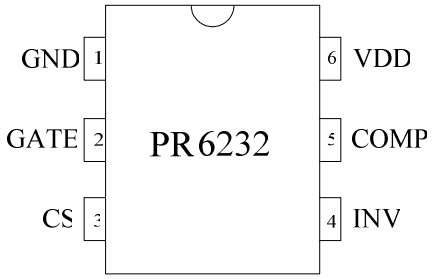


Fig.1. Typical CC/CV Curve

In CC mode, the current point and maximum output power setting can be adjusted by the sense resistor R_S at CS pin. In CV mode, PR6232 captures the auxiliary flyback signal at Pin INV and then regulates the output voltage. IN this mode, multi-mode operations are utilized to achieve high performance and high efficiency. In addition, built-in cable drop compensation further enhances output accuracy.

PR6232 offers power on soft-start control and ensures safe operation with complete protections against all the fault conditions. Built-in protection circuitry includes Cycle-by-Cycle current limiting, peak current protection, VDD OVP, VDD clamp and UVLO. Excellent EMI performance is achieved with frequency jitter and soft-drive.

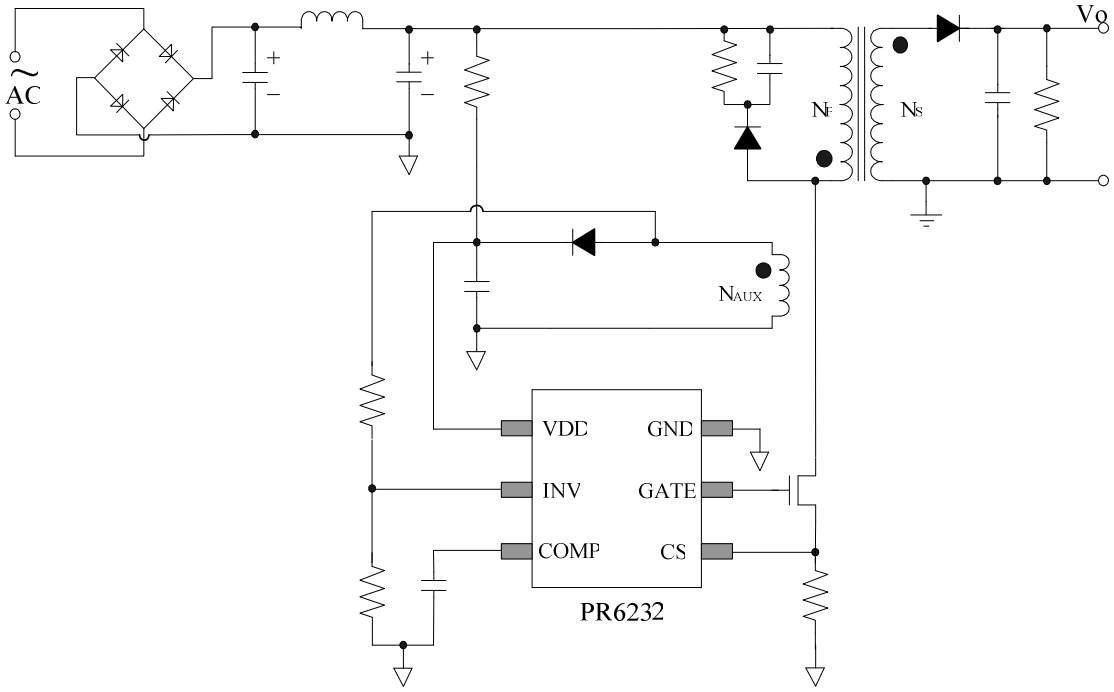
Pin Assignment （SOT23-6 ）



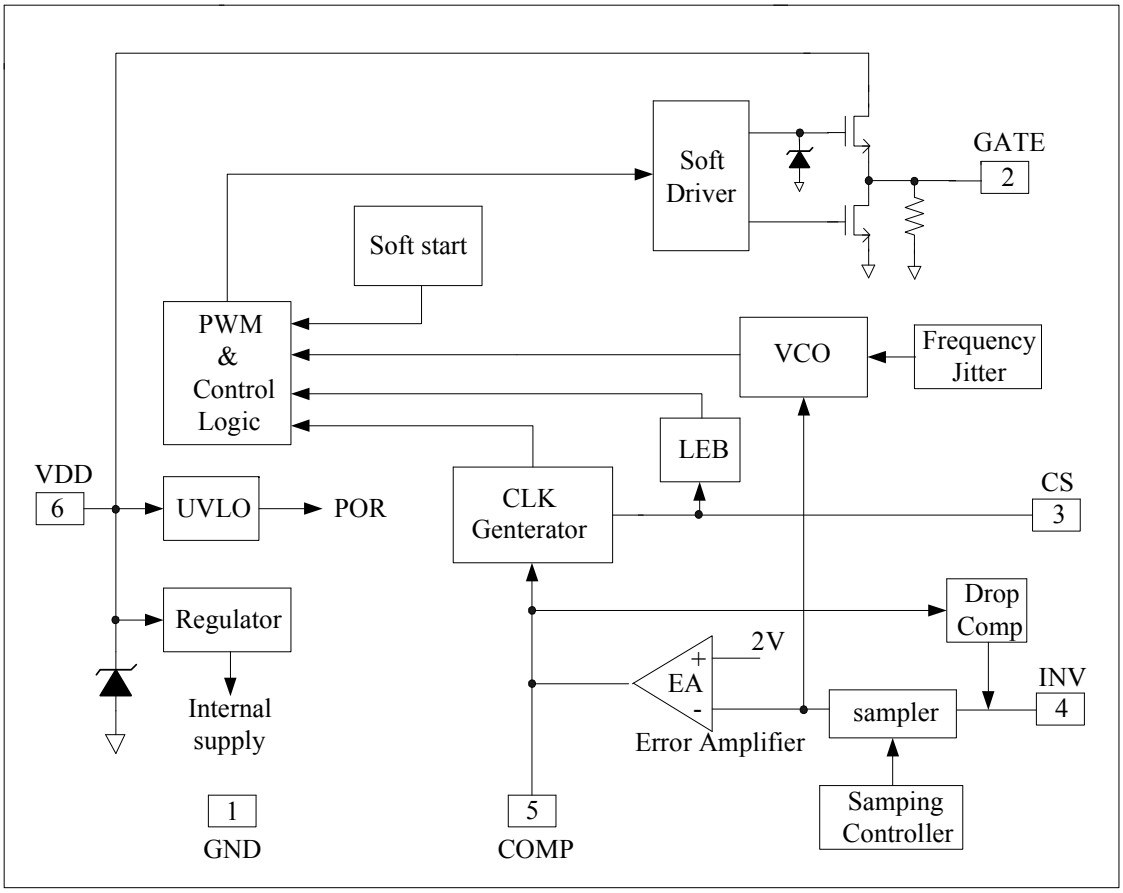
Pin Description

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	GATE	O	Totem-pole gate drive output for power MOSFET
3	CS	I	Current sense input
4	INV	I	The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage. PWM duty cycle is determined by EA output COMP and current sense signal CS.
5	COMP	I	Loop Compensation for CV Stability
6	VDD	P	Power Supply

Typical Application



Block Diagram



Simplified Internal Circuit Architecture

Absolute Maximum Ratings

Parameter	Value
VDD Voltage	-0.3 to VDD_clamp
VDD Zener Clamp Continuous Current	10 mA
COMP Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
INV Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-20 ℃to 150℃
Min/Max Storage Temperature T_{stg}	-55 ℃to 150℃
Lead Temperature (Soldering, 10secs)	260℃

Note: Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Electrical Characteristics

(Ta=25°C unless otherwise noted, V_{DD} = 16V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD) Section						
I_{DD_ST}	Standby current	VDD=13V		5	20	uA
I_{DD_OP}	Operation Current	Operation supply current INV=2V,CS=0V, VDD=20V		2.5	3.5	mA
UVLO(ON)	VDD Under Voltage Lockout Enter	VDD falling	7.5	8.5	10	V
UVLO(OFF)	VDD Under Voltage Lockout Exit	VDD rising	13.5	14.5	16.0	V
OVP	Over voltage protection voltage	Ramp up VDD until gate clock is off	27.5	29.5	31.5	V
V_{DD}_clamp	Maximum VDD opertation voltage	I_{DD}=10mA	30.5	32.5	34.5	V
Current Sense Input Section						
T_{LEB}	LEB time			540		ns
Vth_oc	Over current threshold		870	900	930	mV
Td_oc	OCP Propagation delay			150		ns
Z_{SENSE}_IN	Input Impedance			50		Kohm
T_ss	Soft start time			10		ms
CV Section						
Freq_Nom	System Nominal switch frequency			60		KHz
Freq_startup		INV=0V,Comp=5V		14		KHz
△f/Freq	Frequency jitter range			±4		%
Error Amplifier section						
Vref_EA	Reference voltage for EA		1.97	2	2.03	V
Gdc	DC gain of the EA			60		dB
I_COMP_MAX	Max. Cable compensation current	INV=2V,COMP=0V		42		uA
Power MOSFET Section						
VOL	Output Low level	Io=20mA			1	V
VOH	Output High Level	Io=20mA	8			V
V_clamp	Output Clamp Voltage Level			15		V
T_r	Output Rising Time	CL=0.5nF		650		ns
T_f	Output Falling Time	CL=0.5nF		40		ns

Operation Description

PR6232 is a cost effective PWM power controller for off-line low power AC/DC applications including battery chargers and adaptors. It's designed for the flyback topology working in a discontinuous conduction mode (DCM). It operates in primary-side sensing and provides constant voltage (CV) and constant current (CC) regulation without TL431 and opto-coupler. Built-in secondary constant voltage sampling controller can achieve high precision CC/CV control.

Startup Operation

VDD is the power supply terminal for the PR6232. The startup resistor from the rectified high voltage DC rail supplies current to the VDD bypass capacitor. During startup, the PR6232 typically draws only lower than 20uA, so that VDD could be quickly charged up above UVLO threshold. A large value startup resistor can be used to minimize the power loss in standby mode. As soon as VDD is beyond the UVLO(OFF), the chip will begin to soft-start. It will ramp peak current voltage threshold gradually from nearly zero to 0.90V. This control mode is use to minimize the component electrical over-stress during power on startup. After switching start, the output voltage begins to rise. The VDD bypass capacitor must supply the PR6232 internal circuitry until the output voltage is high enough to sustain VDD through the auxiliary winding.

Principle of CC Operation

PR6232's CC/CV control characteristic is shown as the Fig. 1. PR6232 is designed to operation in DCM mode for flyback system. Under normal operation, when INV is less than 2.0V, the system works in CC mode, otherwise the system works in CV mode.

When the secondary output current reaches a level set by the internal current limiting circuit, the PR6232 enters current limit condition and causes the secondary output voltage to drop. As the output voltage decreases, so does the flyback voltage in a proportional manner. An internal current shaping circuitry adjusts the switching frequency based on the flyback voltage so that the transferred power remains proportional to the output voltage, resulting in a constant secondary side output current profile. This is the CC principle.

In charger applications, a discharged battery charging starts in the CC portion of the curve until it is nearly full charged and smoothly switches to operate in CV portion of the curve.

In PR6232, the CC portion provides output current limiting. PR6232 regulates the output current constant regardless of the output voltage drop in CC operation mode. The CC point and maximum output power can be externally adjusted by external current sense resistor R_S at CS pin as illustrated in Typical Application Diagram. The output power is adjusted through CC point change. The larger R_S, the smaller CC point is, and the smaller output power becomes, and vice versa as shown in Fig.2.

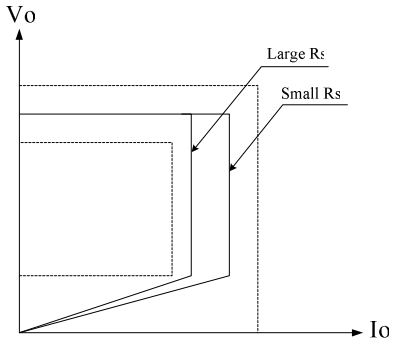


Fig.2. Adjustable output power by changing R_S

Principle of CV Operation

In constant voltage operation, the PR6232 captures the auxiliary flyback signal at INV pin through a resistor divider. The signal at INV pin is pre-amplified against the internal reference voltage. This error signal is then amplified by the internal error amplifier. When the secondary output voltage is above regulation, the error amplifier output COMP decreases to reduce the switch current. Otherwise, the error amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation.

In an AC/DC adapter, the normal operation occurs only on the CV portion of the curve. In CV operation, the output voltage is regulated through the primary side control.

In the DCM flyback converter, the output voltage can be sensed via the auxiliary winding. During MOSFET turn-on time, the load current is supplied from the output filter capacitor C_O, the current in the primary winding ramps up and the energy is stored in the magnetic core of the transformer. When MOSFET turns off, the energy stored in the magnetic core of the transformer is transferred to output.

The auxiliary voltage reflects the output voltage as shown in fig.3 and it is given by

$$V_{AUX} = \frac{N_{AUX}}{N_S} \cdot (V_O + \Delta V) \qquad (1)$$

Where ΔV indicates the drop voltage of the output Diode.

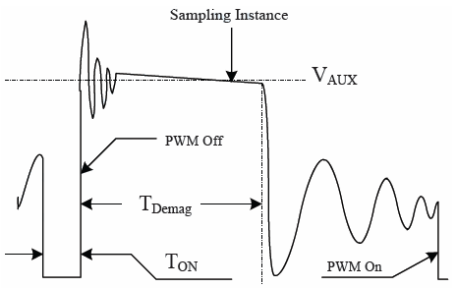


Fig.3. Auxiliary voltage waveform

Via a resistor divider connected between the auxiliary winding and INV (pin 3), the auxiliary voltage is sampled at the end of the demagnetization and it is hold until the next sampling by the internal algorithm control circuit.

The sampled voltage is compared with Vref (2.0V) and the error is amplified. The error amplifier output COMP controls the PWM duty cycle to regulate the output voltage, thus constant output voltage can be achieved.

Program Cable drop Compensation

The voltage drop due to cable loss will increase as the load current increases. It causes the output voltage to fall off. An internal cable drop compensation circuit is designed to compensate the drop due to the cable loss.

When adding to the cable drop, the auxiliary voltage reflecting the output voltage will be corrected comparing with the equation (1). It's given by

$$V_{AUX} = \frac{N_{AUX}}{N_S} \cdot (V_O + \Delta V + V_{cable}) \qquad (2)$$

Where V_{Cable} indicates the drop of the cable.

To compensate the cable drop, an offset voltage is generated at INV by an internal current I_C flowing into the resister divider. The control circuit is shown as Fig.4.

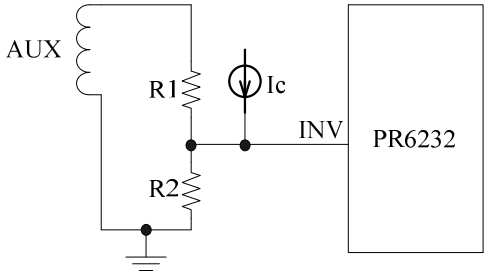


Fig.4. cable drop compensation circuit

The current I_C is inversely proportional to the output COMP of the error amplifier. As a result, it is inversely proportional to the output load current. Thus the drop due to the cable loss can be compensated. The integrate equation is shown as below.

$$V_{ref}(1+\frac{R1}{R2})-I_C R1=\frac{N_{AUX}}{N_S}\cdot(V_O+\Delta V+V_{cable}) \quad (3)$$

As the load current decreases from full-load to no-load, the offset voltage at INV will increase. It can also be programmed by adjusting the resistance of the divider to compensate the drop for various cable lines used. This feature allows for better output voltage accuracy by compensating for the output voltage droop due to the output cable resistance. In PR6232, cable drop compensation is implemented to achieve good load regulation in the CV mode.

Switching frequency

In PR6232, the switching frequency is adaptively controlled by the load conditions and the operation modes. The maximum operation switching frequency is set to 60 KHz internally.

For flyback operating in DCM, The maximum output power is given by

$$Po_{MAX}=\frac{1}{2}L_P F_{SW} I_P^2 \quad (3)$$

Where L_P indicates the inductance of primary winding and I_P is the peak current of primary winding.

The primary-side sensing topology must work in DCM. Refer to the equation 3, to prevent from working in continuous conduction mode (CCM), the switching frequency is locked by an internal loop such that the switching frequency is

$$F_{SW}=\frac{1}{2T_{Demag}} \quad (4)$$

Since T_{Demag} is inversely proportional to the inductance, as a result, the product L_P and F_{sw} is constant, thus the maximum output power is limited.

Current Sensing and Leading Edge Blanking

PR6232 detects primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the cycle-by-cycle current limit. The maximum voltage threshold of the current sensing pin is set as 0.9V. Thus the MOSFET peak current can be calculated as:

$$I_{peak(\max)}=\frac{0.9V}{R_S} \quad (4)$$

A 540 ns leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger caused by the current spike. So that the external R-C filter can be eliminated. The current sense input voltage and the EA output COMP determine the switch duty cycle, and then regulation the output voltage.

EMI improvement

To improve EMI of the PR6232 system, two methods are designed in the chip. One is the frequency jitter. This control is achieved by changing the operation frequency. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI. The other one is soft drive. The internal power MOSFET in PR6232 is driven by a dedicated gate driver for power switch control. Too weak gate drive strength will result in higher conduction and switch loss of MOSFET, while too strong drive will produce EMI problem. A good tradeoff is achieved through the built-in totem pole driver design with right output strength control. The soft drive is designed to open the power MOSFET gradually. In this way, the EMI will be improved much better.

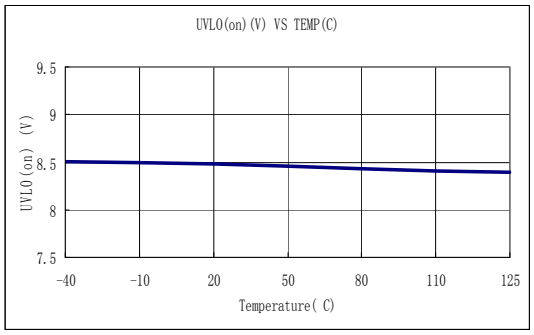
Protection Control

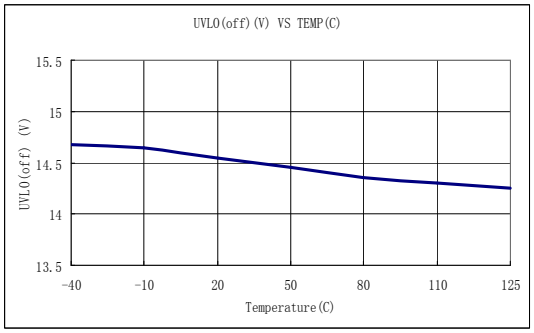
PR6232 ensures safe operation with complete protection against all the fault conditions. When these protections are triggered, the MOSFET will turn off. PR6232 has several protections, such as Cycle-by-Cycle current limiting, peak current protection, over voltage protection (OVP), VDD clamp, power on soft start, and under voltage lockout on VDD (UVLO).

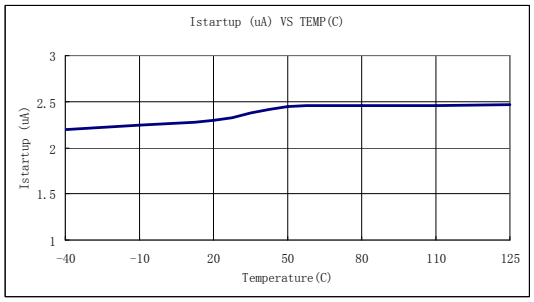
VDD is supplied by transformer auxiliary winding output. The output of PR6232 is shut down when VDD drops below UVLO (ON) limit and then switcher enters power on start-up sequence thereafter. Every restart is a soft-start.

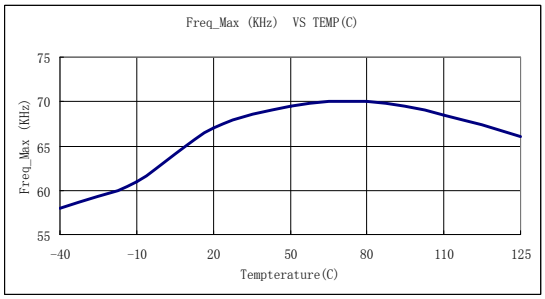
Characterization Plots

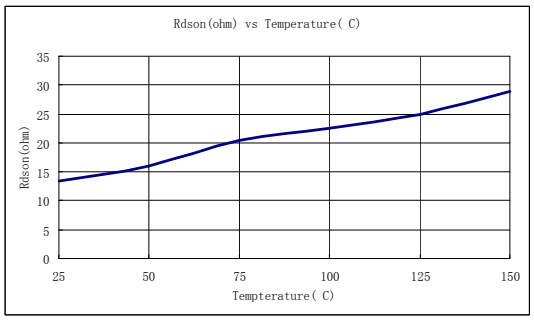
The characteristic graphs are normalized at T_A=25℃.

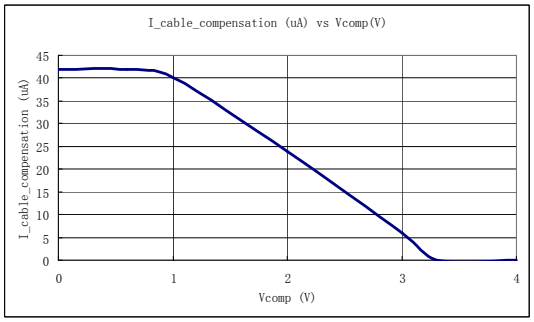






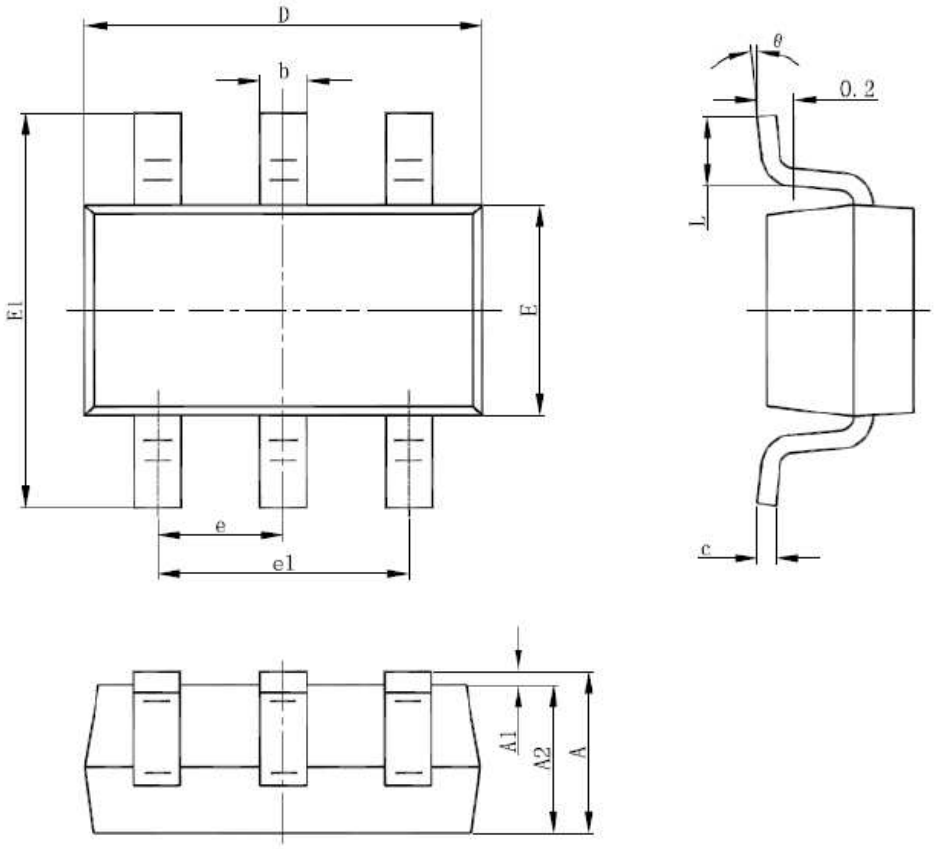






Package Dimensions

SOT-23-6L



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.000	1.300	0.039	0.051
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.095(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ°	0°	8°	0°	8°